Customer No.: 31561
Application No: 10/710,671
Docket No.:13085-US-PA

In the Claims:

Please amend the claims (including new claims 19-22) according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (Currently Amended) A non-volatile memory structure, comprising:

a substrate;

a plurality of gate structures, disposed on the substrate, wherein each ~~substrate~~ gate structure comprises, from the substrate, at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer;

a plurality of select gate structures, wherein each of the select gate structures is disposed on one side of each gate structure respectively such that the gate structures are serially connected together to form a memory cell row, wherein each select gate structure comprises, from the substrate, at least a select gate dielectric layer and a select gate;

a plurality of spacers, disposed between the gate structures and the select gate structures; and

a source/drain region, disposed in the substrate on each side of the memory cell row.

2. (Currently Amended) The non-volatile memory structure of claim 1, wherein said spacers are formed adjacent to and on both sides of each gate structure, wherein there is a space between said spacers not occupied by said gate structures, wherein each of the select gate structures completely fills ~~the~~ said space between ~~the gate structures~~ said spacers.

3. (Original) The non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride.

4. (Original) The non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer and the upper dielectric layer comprises silicon oxide.

5. (Original) The non-volatile memory structure of claim 1, wherein material constituting the control gate and the select gate comprises polysilicon.

6. (Original) The non-volatile memory structure of claim 1, wherein the select gate dielectric layer has a thickness between about 160Å to 170Å.

7. (Currently Amended) A non-volatile memory structure, comprising:

a gate structure, having at least a bottom dielectric layer with a thickness between about 20Å to 30Å, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer over a substrate;

a select gate, disposed on one side of the gate structure;

a spacer, disposed between the gate structure and the select gate;

a select gate dielectric layer, disposed between the select gate and the substrate;

a source region, disposed in the substrate on one side of the gate structure ~~corresponding to~~ opposite the select gate; and

a drain region, disposed in the substrate adjacent to the select gate.

8. (Currently Amended) The non-volatile memory structure of claim ~~1~~ 7, wherein material constituting the charge-trapping layer comprises silicon nitride.

9. (Currently Amended) The non-volatile memory structure of claim ~~1~~ 7, wherein material constituting the bottom dielectric layer comprises silicon oxide.

10. (Currently Amended) The non-volatile memory structure of claim ~~1~~ 7, wherein material constituting the upper dielectric layer comprises silicon oxide.

11-18 (Previously Canceled)

19. (New) The non-volatile memory structure of claim 1, wherein material constituting the cap layer comprises silicon oxide.

20. (New) The non-volatile memory structure of claim 7, wherein the charge-trapping layer of the gate structure has a thickness between about 30Å to 50Å.

21. (New) The non-volatile memory structure of claim 7, wherein the upper dielectric layer of the gate structure has a thickness between about 20Å to 40Å.

22. (New) The non-volatile memory structure of claim 7, wherein the select gate dielectric layer a thickness between about 160Å to 170Å.